

LTCC - a Promising Technology for High-Frequency System-in-Packages

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Abstract:

System-in-Packages (SiPs) are modular packaging solutions comprising one or more semiconductors as well as their passive periphery (capacitors, inductors, resistors, crystals etc.) and interfaces (e.g. sensors). Due to standardised functions and properties these packages simplify the design process for the user. Often-used complex sub-systems are readily available and qualified for a variety of target applications, reducing their design cycle. The SiP (sub-system) itself can evolve independently from the system provided that the interfaces and embedded functions remain. Classical evolutions are triggered by die-shrink due to improved IC-technologies or new requirements for higher functionality maintaining backward compatibility.

LTCC fulfils the requirements of a base material for SiPs. Features as small as 50µm, very good dielectric properties of the glass-ceramics (low dispersion and loss) and controlled layer thickness, provide optimum prerequisites for microwave SiPs. If required the entire module can be hermetically sealed. Multilayer substrates based on LTCC offer the opportunity to print passive components such as resistors, inductors or capacitors on internal layers. The paper focuses on printed capacitors in LTCC for use as decoupling capacitors in a System-in-Package. The best approach in terms of manufacturability is to print a thin layer of high-k-material between electrodes on internal layers. Tolerances, design constraints and rf-properties of embedded capacitors are described and discussed.

Keywords: LTCC, SiP, Passive Integration, Embedded Capacitors, Microwave, High-k-Material

Introduction

Typical candidates for SiPs are RF and microwave applications. Component placement and routing is extremely sensitive for these circuits. In cases where functional trimming is required, it can be accomplished during SiP manufacturing. Implementing chip & wire or flip chip technology tremendously reduces the circuit area compared with discrete solutions using packaged ICs. Shifting of high density wiring from the main board into the SiP also leads to less demanding requirements of the main board resolution, thus reducing the overall system costs. Passives as an integral part of the package offer advantages due to reduced parasitics [1] and size of the system. Additional implemented elements such as sensors and antennae may offer various signal interface options.

A SiP working as a "standardised" sub-system can be applied like a component with defined properties. Further developments or products may use its sophisticated function without considering the typical design constraints necessary for a discrete implementation (Table 1).

Category	Benefit
Reduced Design phase	<ul style="list-style-type: none"> - critical functions are designed only once - usage of these functional blocks does not require detailed subsystem knowledge
Material Cost Reduction at System Level	<ul style="list-style-type: none"> - complex wiring/routing is accomplished within the SiP - the motherboard technology can be simple (layer reduction, via technology)
Reduction of Assembly Costs	<ul style="list-style-type: none"> - critical trimming/tuning steps are made during SiP production (defined performance) - Usage of „known-good packages“ - Reduction of test costs
Miniaturisation	<ul style="list-style-type: none"> - reduced dimensions compared with discrete concepts
Improved electrical Performance	<ul style="list-style-type: none"> - optimised parameters by reducing parasitic effects (short interconnections etc.)
Continuous Product Improvement	<ul style="list-style-type: none"> - Ongoing developments of the SiP does not require system motherboard redesigns (compatibility)

Table 1: Advantages of System in Packages

LTCC SiP with embedded capacitors

The need for embedded capacitors for RF-applications is summarised below:

- Capacitors are required in microwave circuits for different purposes, e.g. coupling / de-coupling, matching, filters, bias networks.
- Smallest SMD-parts qualified for series production are of 0402 size (R&S production line), need space on the surface of a substrate or PCB and have limitations concerning their RF performance due to physical size (electrical length) and mounting technology.
- Integrated printed capacitors on inner layers of the LTCC substrate can significantly reduce the size of the circuit due to true 3D integration and the number of required SMD components. The integrated capacitors offer design freedom in terms of aspect ratio, size and topology. They can therefore be optimized to the required RF performance.
- An RF bias network with capacitor, choke line and 2nd level block with SMD components is a typical application example of such a printed capacitor.

Of the various options to realise embedded capacitors with a high-k material, local printing of a dielectric paste between layers has the best compatibility to existing design procedures and process flow in LTCC. The alternative, to insert entire layers of high-k tapes will adversely affect overall shrinkage and impedance control of interconnections.

Requirements, processing and qualification of a high-k-paste for the Du Pont 951 system have been shown elsewhere [2]. Basic technical data resulting from the use of the dielectric paste are as follows:

- $\epsilon_r = 60-65 @ 1 \text{ MHz}$
- $\tan \delta < 0,01 @ 1 \text{ MHz}$
- Fired thickness: $25\mu\text{m} \pm 4\mu\text{m}$
- capacitance density @ $25\mu\text{m}$: $21\text{pF}/\text{mm}^2$
- Typical capacitance tolerance: $\pm 15\%$
- Material: TiO_2 -based
- Breakdown Voltage @ $25\mu\text{m}$: $> 400\text{V}$
- Electrode metallisation: Ag, Au
- Refire stability tested: 3 post-firings (850°C)
- Temperature behaviour: see Fig. 1

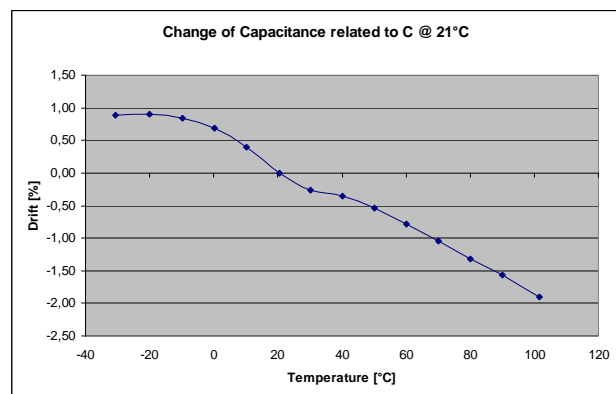


Fig. 1: Relative capacitance drift vs. temperature for embedded high-k-capacitors

Motivation for the fabrication of a capacitor test panel:

The RF performance of the printed capacitors has to be modelled sufficiently well in the simulation tools to achieve an efficient development of complex circuits. 2.5-D planar EM-Simulators (e.g. Sonnet or EM-Sight within Microwave Office) shall be used for this purpose. However, the following technology driven limitations of the printed capacitors were yet to be determined:

- minimum possible size of the electrode plates
- safe contacting of the electrodes by vias without risking short circuits by vias punched through the electrode and the dielectric paste layer during the sintering process of the LTCC
- short circuits due to the electrode material diffusing into micro-cracks in the high-k dielectric layer caused by mechanical stress while sintered
- capacitance per unit area, losses and tolerances of very small capacitors due to fringing fields
- The dielectric loss tangent ($\tan \delta$) resulting from the dielectric paste is specified to be 0.01. However, RF measurements exhibit higher values of $\tan \delta$ depending on the frequency.

A 2.5" x 2.5" LTCC Panel containing 214 test capacitors in different configurations and topologies and with different sizes from $(0.25 \text{ mm})^2$ to $(1 \text{ mm})^2$ was designed and manufactured to verify technological limits, feasibility, capacitance values, RF performance, yield and EM-Simulation quality. 10 of these panels have been produced, 5 of them have been measured and analysed. The resultant different topologies of printed capacitors used on the test panel are described:

Type 1 (shunt capacitor, Fig. 2):

- SMD components or dice can be placed directly above on the surface, offering low parasitic inductance
- Bottom electrode is connected by 1 via (type 1a) or 4 vias (type 1b)

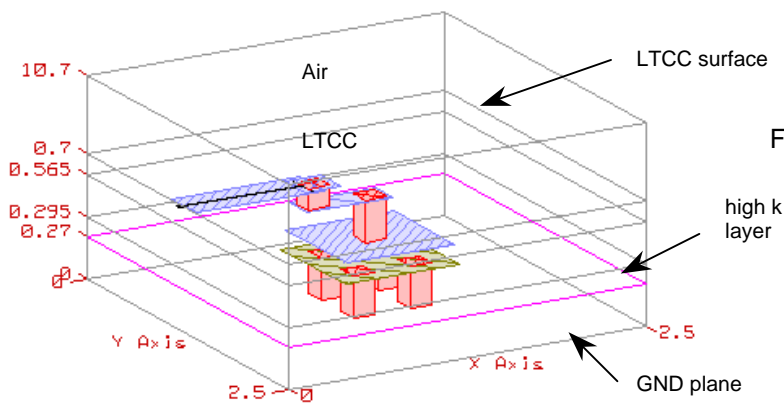


Fig. 2: Type 1b capacitor design

Type 2 (vertical shunt capacitor with buried feed line, Fig. 3)

- SMD components or dice can be placed directly above on the surface
- Bottom electrode is connected by 1 via (type 2a) or 4 vias (type 2b)

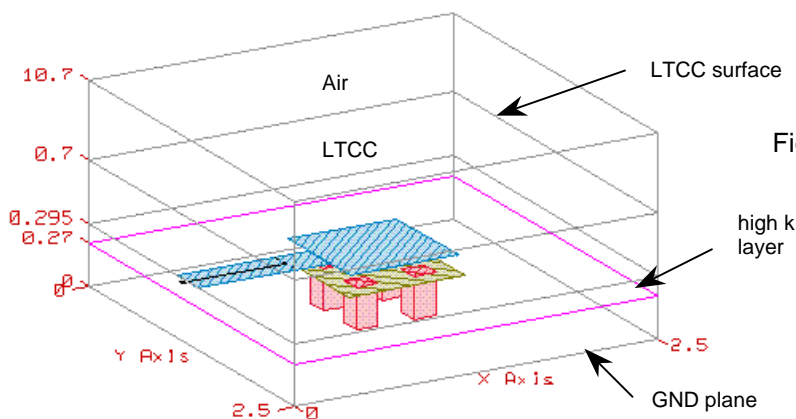


Fig. 3: Type 2b capacitor design

Type 3 (series capacitor, Fig. 4)

- used, if direct contacting by vias is not possible
- safest design in terms of reliability
- highest parasitic inductance compared to type 1 and 2

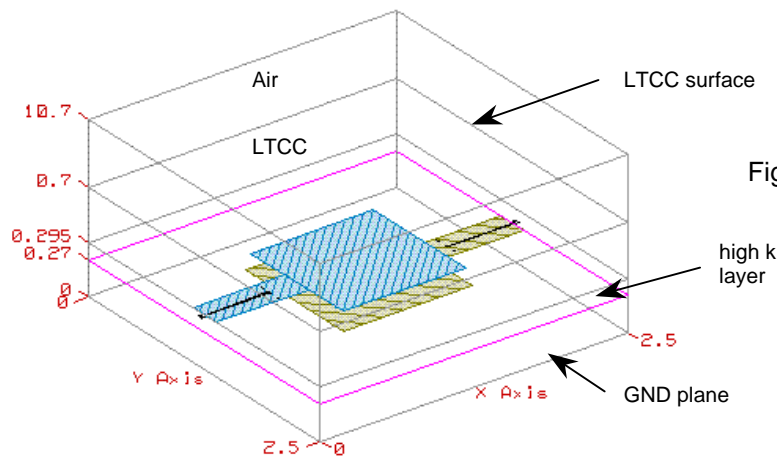


Fig. 4: Type 3 capacitor design

Measurement Results:

The measured properties of the capacitors are capacitance, resonance frequency and loss as well as tolerances and spread of each of these characteristics.

Measurement setups:

- All measurements were performed on an on-wafer prober with on-wafer probes in 800 μm -pitch GSG configuration.
- Each capacitor is connected by a feed structure, which is exactly half of the symmetrical through standard of the appropriate TRL (Through, Reflect, Line) calibration kit on the same LTCC panel. The calibration kit was designed to cover the frequency band from 1 to 8 GHz.
- RF characteristics such as resonant frequency and loss were measured with a network analyser calibrated with TRL calibration to de-embed the feed structure between the on-wafer probe pads, where the probe tips make contact, and the actual capacitor. Thus the reference plane of the RF measurements is moved to the edge of the electrode plate or to the via contacting the electrode from the top. Full one or two port S-Parameters between 1 and 8 GHz have been recorded from each capacitor.
- Capacitance was measured with a network analyser calibrated with a TOSM (Through, Open, Short, Match) calibration on a calibration substrate. Measurement frequency was 50 MHz, so that the electrical length of the feed structure between the on-wafer probe pads, in the TOSM calibration reference plane, and the actual capacitor had negligible effect on the result. Nevertheless, in order to achieve best possible accuracy, the capacitance of this feed structure, which is needed for the RF measurements with TRL calibration, has been measured and deducted from the results.
- Series resistance was determined at the series resonance from the S-Parameters.
- A value of dielectric loss tangent ($\tan \delta$) was fitted to the data, so simulated S-Parameters match the measured ones for the real part of the input impedance over the complete frequency range 1 – 8 GHz.

S-Parameter Results:

A typical RF measurement result is shown in the graph below (Fig. 5) for the largest capacitor of the test coupon. The simulation data exhibit good agreement with the measured results. A dielectric loss tangent of the paste material of $\tan \delta = 0.04$ was assumed. A larger deviation between the measured and simulated behaviour was obtained for the smallest capacitor. Due to the smaller than expected capacitance value, the self resonance frequency was measured to be much higher than simulated.

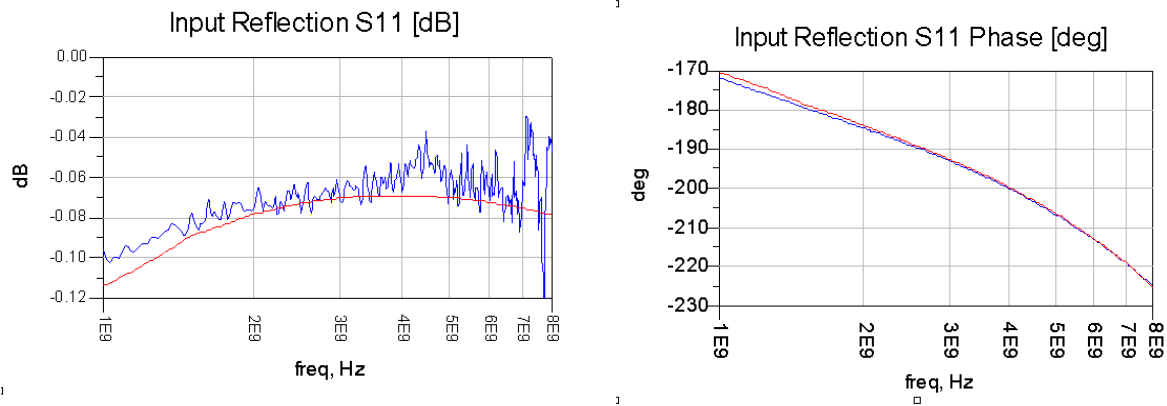


Fig. 5: S-parameter measurement (blue) and simulation (red) results for a 1mm² shunt capacitor (1-port)

Capacitance values:

The following Table 2 contains the measurement results for the capacitance values of all printed capacitors of the topology type 2a from 0.25 mm to 1 mm electrode edge length. The results are compared with the simulation data and displayed graphically in the diagram in Fig. 6. This diagram also shows the curves for the series of measurements of the capacitors of the topology type 1b with 4 vias to GND from the bottom electrode. Each series consists of 20 samples on 5 different wafers.

Capacitor parameter	1	2	3	4	5	6	7
electrode edge length [mm]	0.25	0.30	0.35	0.40	0.50	0.75	1.00
electrode area [mm ²]	0.063	0.090	0.123	0.160	0.250	0.563	1.000
mean capacitance [pF]	1.29	1.97	2.95	3.89	6.10	13.95	25.04
maximum capacitance [pF]	1.41	2.20	3.26	4.15	6.42	14.14	25.25
minimum capacitance [pF]	1.13	1.81	2.66	3.55	5.82	13.80	24.89
standard deviation [%]	9.65	8.85	5.43	5.17	3.66	1.07	0.61
maximum deviation [+/-%]	11.10	9.99	10.20	7.62	4.95	1.22	0.70
simulated capacitance [pF]	1.87	2.53	3.30	4.18	6.29	13.50	23.51
difference measurement - simulation [%]	-30.8	-22.2	-10.5	-7.0	-3.0	3.3	6.5
max. deviation from simulation [%]	41.9	32.2	20.7	14.6	8.0	4.6	7.2
measured capacitance per unit area [pF/mm ²]	20.7	21.8	24.1	24.3	24.4	24.8	25.0
simulated capacitance per unit area [pF/mm ²]	29.9	28.1	26.9	26.1	25.1	24.0	23.5

Table 2: Measured and simulated capacitance values for various capacitor sizes

The graphic in Fig. 7 presents the capacitance distribution over different wafers. It appears that the mean capacitance per unit area value can vary from wafer to wafer about $\pm 5\%$.

The results indicate that the spread of the capacitance values increases significantly with decreasing electrode area (see standard and maximum deviation in the table). The measured capacitance per unit area of the capacitor type 2a declines with decreasing electrode area and drops considerably below 0.1 mm². This is contrary to the simulation results, which exhibit an increasing capacitance per unit area towards smaller electrode areas due to fringing fields. One potential reason for this effect could be attributed to the screen printing process. Smaller areas tend to be thicker compared to larger ones. Similar effects are known to occur in thick film resistors.

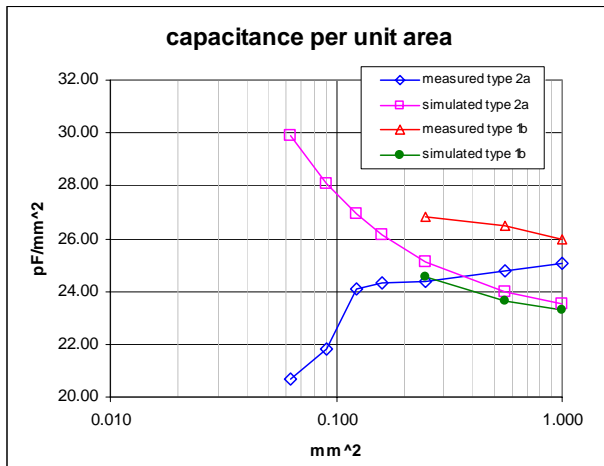


Fig. 6: Comparison of measured and simulated capacitance values

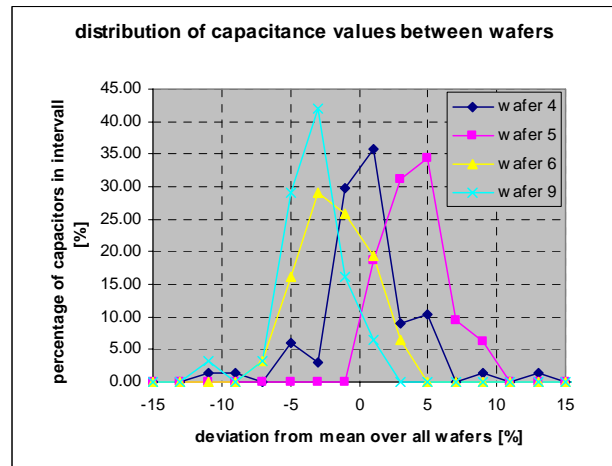


Fig. 7: Capacitance deviation on different test substrates

Self Resonant Frequency and Series Resistance:

The left graph below (Fig. 8) shows the series resonant frequency achieved with the printed capacitors of the topology type 1a. If the bottom plate is connected to the ground plane by 4 vias instead of one (type 1b), a slight increase of the resonant frequency about 200 MHz can be seen. Furthermore the series resistance at the resonant frequency will drop about 30% as displayed in right graph below (Fig. 9). But 4 vias can be used only at electrode edge lengths above 0.5 mm.

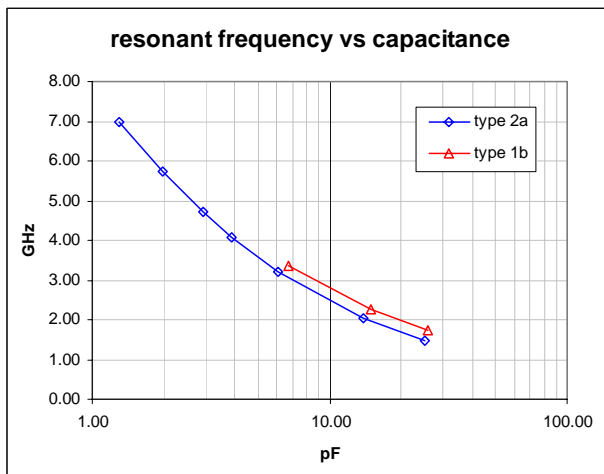


Fig. 8: Impact of electrode size on self resonance frequency

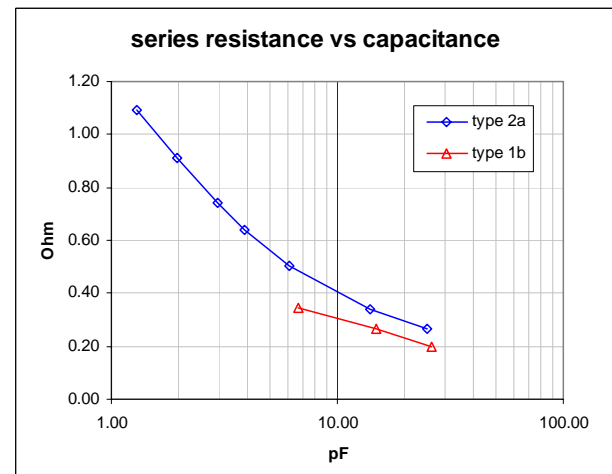


Fig. 9: Impact of electrode size on series resistance

In comparison with 0402 SMD components (e.g. Murata GRM1555C series), the measured self resonant frequencies are about 30% higher. The spread of the measured resonant frequencies of the 20 samples on all 5 wafers for one capacitor size and topology is about $\pm 6\%$ if the topology is of type 2 or 3 and about $\pm 3\%$ if the topology is of type 1. If the resonant frequency is displayed over capacitance for simulation and measurement in comparison, it appears that the simulation is 100 to 200 MHz lower than actually measured. This applies for all topologies and configurations.

The measured series resistance varies up to $\pm 25\%$ among the samples of one specific capacitor. The difference between the mean of all measured values and the simulation can be up to 30%.

The quality factors of the printed capacitors vary between 15 and 20 depending on topology and size. For comparison, the quality factors of standard SMD capacitors of 0402 size are about 30 to 40. Hence losses leave room for improvement.

Dielectric loss tangent of high-k paste material:

The dielectric loss tangent ($\tan \delta$) of the high-k paste used for the printed capacitors apparently depends on the frequency. Simulation with $\tan \delta = 0.04$ instead of 0.01 gives good agreement with TRL calibrated RF measurements, but at lower frequencies the TOSM calibrated measurements show lower loss. Simulations applying $\tan \delta = 0.02$ fit measurements between 50 MHz and 1 GHz well.

Conclusion:

The measurements discussed in this paper have proven that printed ceramic capacitors within LTCC structures can be used for the desired applications (coupling / decoupling, mainly in bias networks). They have higher resonant frequencies but lower quality factors than 0402 SMD capacitors. The higher loss compared with 0402 SMD components is no major drawback for the intended application. While the overall RF performance of the printed capacitors is comparable with 0402 SMD components, the integration capability offers an important benefit of printed capacitors. Thereby a compact design and advantages for RF performance (e.g. short interconnects) can be realised. It has to be considered that the RF performance of the SMD capacitors in the comparison was based on plain components without solder pads. Solder pads can degenerate the RF performance.

Reference:

[1] Takeshi Hanawa, Ilkka Urvas: "Comparison of LTCC Passive Components in Different Structure", Proceedings of 2003 ICEP (International Conference on Electronics Packaging) organised by IMAPS Japan and IEEE CPMT Society Japan, April 16-18, 2003, Tokyo.

[2] J. Müller, D. Josip, "Integrated Capacitors using LTCC", in *Proceedings of MicroTech 2002*, Manchester/UK, January 2002