Wafer Scale CSP Technology: Design, Substrate and Manufacturing Requirements

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Abstract

Today's routing density and semiconductor contact pitch requirements forces designers to develop effective packaging solutions which provide the thermal, electrical and mechanical performance desired for their products. This rapid evolution towards substantially higher I/O counts drives the adoption of new interconnection strategies at the board level. In general, chip I/Os cannot be distributed by peripheral leads around the circuit edges while maintaining a practical pitch. One popular approach addressing this issue is to use the chip's entire surface area to enable a coarser pitch area array of interconnections thereby providing a wafer scale Chip Scale Package (CSP) with thin film redistribution. The market for such micro-packaging technologies is currently driven by memory manufacturers and is becoming increasingly accepted for a variety of product applications (e.g. camcorder, notebooks, mobile phones etc.).

The customized design of CSPs provides considerable advantage to circuit manufacturers. CSPs are more immune to die changes (e.g. shrinkage of die area) and thus provide users an option to accommodate future die shrinks early in the design phase. The design of a CSP can in turn impose extreme requirements on the associated substrate design. The CSP land pad pitch should be standardized to allow die testing using commercially available contactor solutions. Solder bump pitch and pad diameter also define the specific needs of component placement. In addition, the pad pitch determines the number of layers required to fan out the signals on the substrate using a given line resolution capability. All these issues need to be addressed early in the design phase to minimize overall product cost. For all of the above reasons, wiring density is a decisive factor in the selection of the substrate technology. During the past five years a tremendous increase in wiring density has been achieved by High-Density-Interconnect (HDI) substrates based on microvias in organic laminates. Other solutions are offered by either HTCC or LTCC with the built in capability of small, stacked vias.

From an assembly perspective, the major advantage of wafer scale CSPs and flip chip assembly over the more traditional chip and wire hybrid assemblies is their compatibility with standard surface mount assembly processes thereby enabling a single step assembly process. Standard surface mount devices can be placed along with CSPs and reflowed simultaneously, minimizing processing time. This paper describes the capability and advantages of wafer scale CSPs and discusses the board technology and automated assembly process requirements required to successfully deploy this technology.

1. Chip Scale Packages – CSP

What characterizes a CSP? The most common definition of a chip scale or chip size package is that the outline of this area array package should not extend the outline of the bare die by a factor more than 1.2 or in other words the area should not be greater than 1.5. Today there are more than 50 different packages available that more or less satisfy this definition. Despite this proliferation of CSP options, they all can be classified into on of 3 major subgroups:

a) rigid interposer CSP (wire bond or flip chip)
b) flex interposer CSP (wire bond or flip chip)
c) wafer level CSP

Rigid interposer based CSPs can be further sub-classified into ceramic and organic carrier subcatagories.

The third class of CSPs is called wafer level CSPs (WL-CSPs). The main differentiator of this CSP approach is the processing of the integrated circuits at the wafer level. This batch process is expected to result in cost savings over the other serially processed packages. More recently the lines have blurred between flip chip and WL-CSPs since both processes generally involve the use of an additional thin film metal redistribution layer. The differences between these two packaging technologies are largely semantics and are basically related to bump pitch. Most of today's flip chip applications involving bump pitches below 300 microns and whereas WL-CSP pitches are generally in the 300 to 800 micron pitch range. To date pitches of 0.8 mm and 0.5 mm have been most popular as they provide a much broader assembly process window. Since all of the I/O's for a given die size must be accommodated within the individual die area smaller pitches such as 350 µm, 300 µm or even 250 µm are expected in the next few years in order to accommodate higher I/O, more dense integrated circuits. Which factors should be considered in the selection of a CSP? Cost, reliability and process / product compatibility are usually the most important considerations. Some important properties which are defined by the product and its environment are summarized in Table 1.

Mechanical/thermal	Electrical	Technological
- area available - max. component height - requirement of underfill - working conditions (temp. Range etc.) - TCE - Thermal conductivity - Moisture uptake	- Testability as CSP - line inductance - line capacitance - line resistance - cross talk - power requirements	- placement accuracy (CSP-pitch, bump-diameter) - I/O density on CSP (wiring density) - max. routable number of bump rows (board) - reworkability (CSP change)

Table 1: Important considerations in CSP selection.

In terms of maximum exploitation of space (both area and component height) WL-CSPs offer the best solution. Most WL-CSP technologies available today are based on simple thin film redistribution and wafer bumping processes. Although some favorable reliability claims have appeared in the literature, it is unlikely that adequate reliability will be obtained over a broad range of die size, I/O count and substrate material unless an underfill process is used to ruggedize the assembly. The longer term goal of WL-CSP efforts in the industry is to build in compliancy into the package so as to decouple the IC from the substrate thereby providing adequate board level reliability while at the same time avoiding underfill.

2. Advantages and Disadvantages of CSPs

The highest potential of WL-CSPs lies in their compatibility with conventional surface mount processing. This is especially the case if pitches of 0.5 mm or greater can be maintained. Compared to leaded perimeter packages like QFPs, high assembly yields are possible because of the inherent self-alignment capabilities of area array solder connections which effectively reduces component placement error (X,Y, theta) sensitivity. Like BGAs, CSPs are self centering during reflow due to the wetting behavior and surface tension of the solder. Unlike COB interconnection processes, CSP interconnections are made in parallel thereby dramatically reducing process cycle time. In addition to this time, COB approaches also suffer from the vulnerability of wire connections prior to glob top application and cure.

With enough forethought CSPs can be designed to incorporate predictable die shrinks (Figure 1). Alternatively, the CSP I/O footprint can already include further functions of a circuit family. Later required interconnections are integrated in the CSP pad structure serving as place holders (Figure 2). Both the CSP redistribution and the board layout need no further configuration when introducing the next circuit generation affording tremendous reduction in the development cycle.

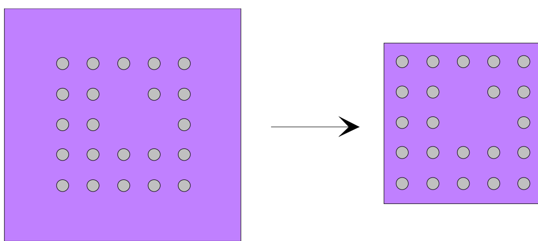

Fig. 1: Die shrink capability of CSP designs

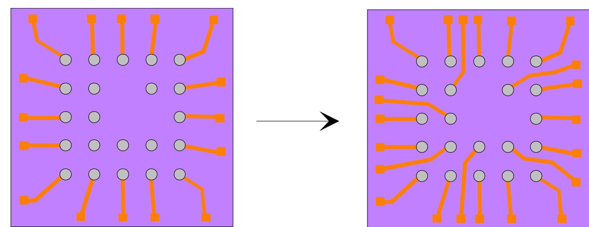

Fig. 2: Upgrade capability of CSP designs

On the other hand, the infrastructure needs to be adapted for direct chip attach. X-Ray equipment is mandatory for solder joint evaluation, especially during process optimization efforts. In most applications, CSPs require underfill to increase product reliability.
The latter increases the keep out area required to apply the underfill. When compared to his wire bonded pendant there is almost no reduction of area occupied if wire bonds can be drawn in a single row (Figure 3). However, the actual situation is dependent on bare die dimensions, bond pad pitch, number of I/O and the keep out area for rework and underfill. If rework is not intended two or more CSPs can be placed edge to edge occupying far less space than wire bonded ICs by saving the keep out areas (Figure 4). In those applications where such demanding space constraints exist, the underfill dispense flow needs to be optimized for this configuration.

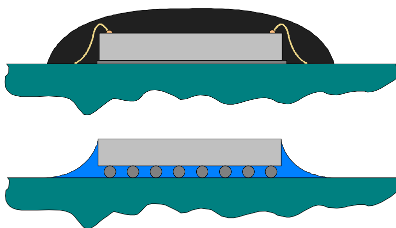

Fig. 3: Area comparison COB vs. CSP

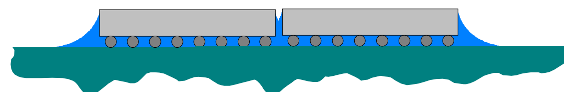

Fig. 4: Best area exploitation by close placement

3. Wafer Level CSPs

The redistribution structure on wafer level CSPs is built up using thin film processes. Lines are made by aluminum or copper with trace widths ranging from 10 µm to 50 microns. The line structure can be deposited directly on the chip passivation or on an additional passivation coating the primary chip passivation (Figure 5). A second passivation with windows for the CSP pads

protects the conductor traces and serves as a solder mask. Prior to solder bumping the pad metallization is provided with an under bump metallization (UBM) e.g. Ni/Au. Bumps can be applied by solder paste printing [1], sputtering or placing of preformed bumps and additional reflow. The complete process is described in [2]. Figure 6 shows such a wafer level CSP with a contact pitch of 0.5 mm and 150 µm bumps. Since all steps are carried out in the wafer format (parallel for all dice at a time) this process offers cost benefits compared to other CSP technologies. Testing of CSPs can be completed in the wafer form prior to singulation.

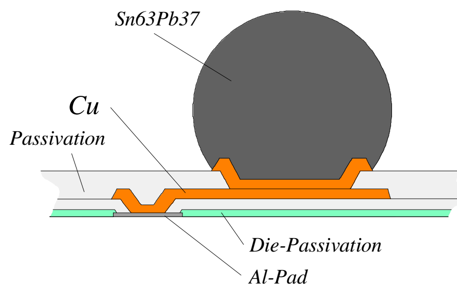

Fig. 5: Typical construction of a WL-CSP

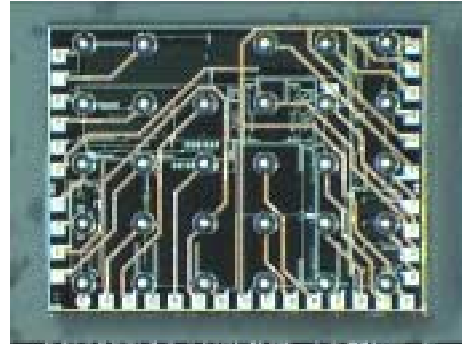

Fig. 6: WL-CSP with 0.5 mm pitch

Since the area available for the pad array is limited by the dimension of the bare die, the required CSP pitch is directly related to the minimum bond pad pitch desired and number of I/O required for a given IC. Considering die fully populated with bond pads on the perimeter, the number of I/Os is a linear function of the die area. It is obvious that the advantage of CSPs becomes more and more evident with growing die size. Figure 7 shows the relation between bond pad pitch and CSP pitch (of a fully populated array) with the die size as parameter. Extremely small dice with a tight bond pitch are pushing this technology to its limits. However, in reality the effective number of I/O in most applications is much smaller relaxing this situation.

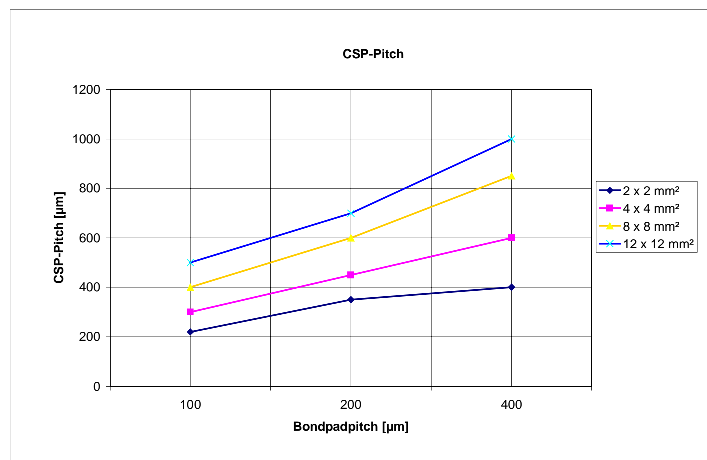

Fig. 7: CSP pitch vs. Wire bond pitch

4. Requirements on substrate technology

Though CSPs enable the use of more moderate pitches compared to the traditional perimeter fan-out requirements, they also impose quite demanding wiring density requirements. Especially the inner signals of an area array pad arrangement are difficult to route. They need to be drawn to inner layers if the channel capacity between pads is not sufficient for all lines. This effect becomes decisive with reduced CSP-pitches. The worst case – no line possible between two pads – requires a separate layer for each signal row.

Due to the use of small solder bump diameters (less than 150 microns) for WL-CSPs, substrate flatness is an important yield determining factor in manufacturing. The key parameters are:

- Initial substrate warpage ≤ 1%
- No bending, twisting during thermal treatment (reflow, underfill curing)
- Coplanarity of CSP pad array.

All properties can and must be addressed in the substrate design. The first two parameters can be maintained with symmetrical board constructions compensating TCE mismatches between different materials in a laminate. If necessary boards need to be kept flat during reflow by means of special tooling. Coplanarity of adjacent pads of a build-up structure is controlled by the underlying layers. If it is necessary to guide conductor traces directly under certain pads the remaining areas under pads should be filled with metal as well (Fig. 8).

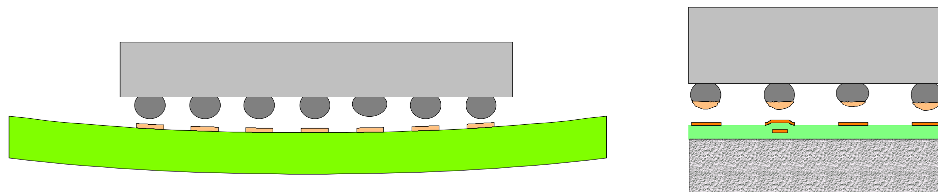

Fig. 8: Possible solder failure sources caused by warped substrate or improper design

4.1 Organic substrates

During the past years an increasing number of High-Density-Interconnect (HDI) technologies based on photo-, laser- or plasma-defined microvias have been developed. Typical materials applied for these boards are polyimide and RCC-foils (resin coated copper). Traces can be fine-line structured down to 50 µm. However, the decisive parameters for CSP-designs are the size of the via catch pads and the alignment of the solder mask to the conductor pattern. Both properties are dictated by process tolerances. Figure 9 and Table 2 show CSP-relevant dimensions for microvia boards.

	Parameter	**Standard**	**Advanced**
a)	Line width	125 µm	50 µm
b)	Line space	125 µm	50 µm
c)	Keep out solder mask = positioning tolerances to conductor pattern	75 µm	50 µm
d)	Min. width solder mask	120 µm	75 µm
e)	Min. overlap Solder mask	100 µm	60 µm
f)	CSP-landpad	200 µm*	150 µm*
g)	Via-catchpad	350 µm	200 µm

*) dependent on solder bump diameter

Table 2: CSP-relevant design parameters for organic substrates

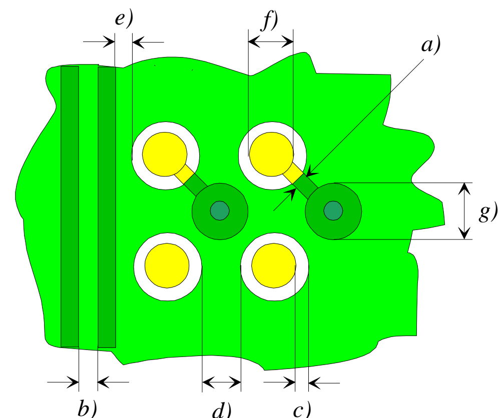

Fig. 9: CSP-pad design

Due to the microvia-generation stacked vias are not possible on most HDI technologies. Therefore, additional space will be occupied for buried vias on inner layers reducing the wiring density and the number of routable CSP pad rows. Figure 10 shows case studies for CSP pitches of 0.5 mm and 0.35 mm. Signal distribution is achieved on both examples using two layers. However, the number of pad rows is limited to four at the 500 µm CSP and three at the 350 µm CSP respectively. The solder pads for the CSP may be solder mask or non-solder mask defined.

If not electrically required (shielding etc.) designers should focus on minimizing the number of build-up layers. This is on the one hand cost-effective and on the other hand, the best way to meet the surface topology requirements mentioned above.

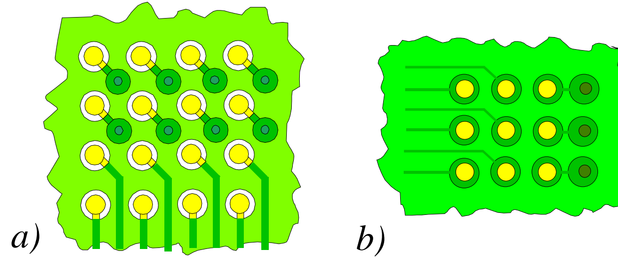

Fig. 10: Fan out of CSP-pads for a) 500 µm pitch   b) 350 µm pitch

4.2 Ceramic substrates

Substrates based on LTCC or HTCC can take advantage of stacked vias. Signals going down three layers or more directly under the CSP pad are feasible. A separate solder mask is not necessary. Table 3 contains a list of parameters influencing the capability of CSP-designs. Fig. 12 demonstrates the potential of multilayer ceramics for CSP applications. Even with relaxed design rules it is possible to route fine pitch CSPs using additional layers. The total number of layers is a cost determining factor in multilayer ceramic substrate design. However, a minimum number of four layers is typically required to achieve the desired substrate stability. Reduction of layers necessary is easily obtained by taking advantage of the fine line resolution of cofire conductors on green sheets. Line widths and spaces of 100 µm are reproducible. It has been demonstrated to achieve even a 50 micron line width in selected areas [3].
Due to the excellent TCE match between LTCC and die, the reliability of these interconnects is very high [4].

	Parameter	**Standard**	**Advanced**
a)	Line width	150 µm	75 µm
b)	Line space	150 µm	75 µm
c)	Via-diameter	130 µm	90 µm
d)	min. Via-pitch	350 µm	250 µm
e)	Via-catchpad (postfire) Via-catchpad (cofire)	250 µm 200 µm	180 µm 140 µm
f)	max. number of stacked Vias	3	6
g)	Number of layers	4-6	8-10

Table 3: Design parameters LTCC/HTCC

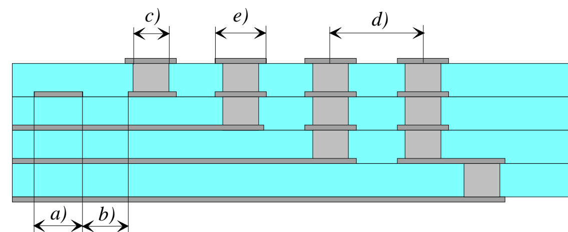

Fig. 11: CSP-relevant dimensions

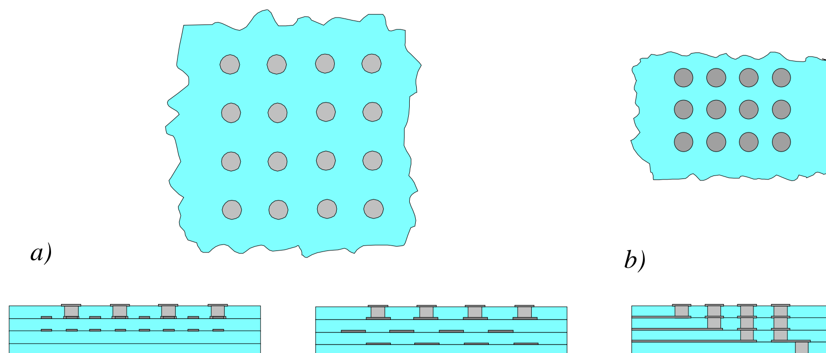

Fig. 12: Fan out of CSP-pads for a) 500 µm pitch   b) 350 µm pitch

5. Requirements on assembly technology

The main advantage that WL-CSP assembly has over more aggressive fine pitch, flip chip assembly is the relief that it affords to both the interconnecting substrate requirements and assembly needs. The placement accuracies of most surface mount "state of the art" pick and place tools that are capable of placing bare die typically range in the 15 to 30 micron range. For pitches of 500 microns or greater, placement tolerances of about half of the pad diameter is possible due to the self-allignment capabilities of area array solder connections. Consequently most competitive pick and place tools available today can be used for assembly. Our intent in developing and implementing such a coarse pitch assembly technology has been to enable the incorporation of bare die assembly into general surface mount assembly with a minimal amount of difficulties. This makes placement of WL-CSPs a very high yielding process with defect rates on a per joint basis of well below 5 ppm. The use of relatively large solder ball diameters makes underfilling of the die very straightforward, and eliminates most of the obstacles that seem to plague finer pitch, lower stand-off flip chip assembly. Issues such as shadow voiding during underfill flow, segregation of underfill particles during the underfill process are also generally not observed. Although post-underfill rework is not possible, the ruggedness of these larger solder connections affords the robustness to the assembly that enables full electrical test prior to underfill. Although the elimination of the underfill process remains a key goal in the development of WL-CSPs, in the meantime the ease of undefilling these assemblies makes it quite practical in high volume manufacturing despite the inconveniences.

6. Acknowledgement

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